standard." This is in contrast to other classes of analog integrated circuits such as operational amplifiers, regulators, or multipliers which have gained wide customer acceptance.

There are three basic limitations to integrated active-RC filters techniques: (1) frequency range: stability considerations limit the use of most of these filters to below 100 kHz; (2) sensitivity: the selectivity and the center frequency are often very sensitive functions of active gains or absolute values of feedback components; (3) cost: typically four precision components (two R's and two C's) are required for each complex pole pair. These components can only be fabricated in integrated form using thin-film and hybrid technology, thus adding to the cost and complexity of design.

In certain applications, it is possible to overcome some of these disadvantages of active-RC filters by using alternate design approaches which differ significantly from the basic linear feedback techniques described so far. One specific example of such an approach is the use of a phase-locked loop (PLL) system to obtain desired selectivity function. This is described in the second part of this chapter.

PART II Phase-Lock Techniques

9.10 THE PHASE-LOCKED LOOP (PLL)

In the design of frequency selective integrated circuits using phase-lock techniques, one utilizes the frequency selective signal processing properties of a phase-locked loop (PLL) system. The basic concept of a PLL has been known since the early 1930's. However, due to its cost and complexity in nonintegrated system design, the application of the PLL has been limited to precision measurements requiring a high degree of noise immunity and very narrow bandwidths.

Figure 9.15 shows the block diagram of a basic phase-locked loop system. The PLL is a feedback system comprised of a phase comparator, a low-pass filter and an error amplifier in the forward signal path, and a voltage controlled oscillator (VCO) in the feedback path. A detailed analysis of the PLL as a quasi-linear feedback system is available in the literature [24,25] and will not be repeated here. However, from a qualitative point of view, the basic principle of operation of a PLL can be briefly explained as follows: With no signal input to the system, the error voltage, $v_d(t)$ of Fig. 9.15, is equal to zero. Then the VCO operates at a set fre-

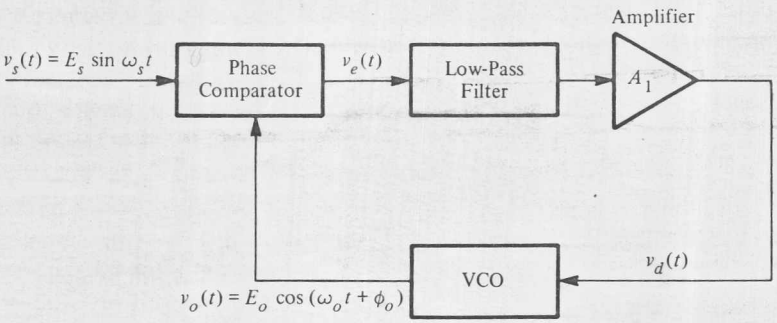


Figure 9.15 Block diagram of a phase-locked loop (PLL) system.

quenty, $\omega_0 = 2\pi f_o$, known as its "free-running frequency." If an input signal, $v_s(t)$, is applied to the system, the phase comparator compares the phase and the frequency of the input with the VCO frequency and generates an error voltage, $v_e(t)$, related to the frequency and the phase difference between the two signals. This error voltage is then filtered, amplified, and applied to the control terminals of the VCO. In this manner, the control voltage, $v_d(t)$, forces the VCO frequency to vary in a direction which reduces the frequency difference between f_0 and the input signal. If the input frequency f_s is sufficiently close to f_0, the feedback nature of the PLL causes the VCO to synchronize or "lock" with the incoming signal. Once in lock, the VCO frequency is identical to the input signal, except for a finite phase difference. This net phase difference ϕ_o is necessary to generate the corrective error voltage v_d to shift the VCO frequency from its free-running value to the input signal frequency f_s, and thus keep the PLL in lock. This self-correcting ability of the system also allows the PLL to "track" the frequency changes of the input signal once it is locked. The range of frequencies over which the PLL can *maintain* lock with an input signal is defined as the "lock range" of the system. This is always larger than the band of frequencies over which the PLL can *acquire* lock with an incoming signal. This latter range of frequencies is known as the "capture range" of the system.

The capture process is highly complex, and does not lend itself to simple mathematical analysis. However, a heuristic and highly qualitative description of the capture mechanism may be given as follows: Since frequency is the time derivative of phase, the frequency and the phase errors in the loop can be related as:

$$2\pi\Delta f(t) = \gamma \frac{d\phi_o(t)}{dt} \tag{9.46}$$

where $\Delta f(t)$ is the instantaneous frequency separation between the signal and the VCO frequencies, and γ is a constant of proportionality.

If the feedback loop of the PLL were opened, say between the low-pass filter and the VCO control input, then for a given setting of f_0 and f_s the phase comparator output would be a sinusoidal beat-note at a fixed frequency Δf. If f_s and f_0 were sufficiently close in frequency, then this beat-note would be passed by the low-pass filter, with negligible attenuation. Now suppose that the feedback loop is closed by connecting the low-pass filter output to the VCO control terminal. Then the VCO frequency would be modulated by the beat-note, and when this happens, Δf itself becomes a function of time. If during this modulation process, the VCO frequency moves closer to f_s (i.e., decreasing Δf), then $(d\phi_o/dt)$ decreases and the output of the phase comparator becomes a slowly varying function of time. Similarly if the VCO is modulated *away* from f_s, $(d\phi_o/dt)$ increases and the error voltage becomes a rapidly varying function of time. Therefore, under this condition, the beat-note waveform no longer looks sinusoidal; instead it looks like a series of aperiodic "cusps," shown schematically in Fig. 9.16. Because of its assymetry, the beat-note waveform contains a finite dc component which pushes the "average" value of the VCO toward f_s, thus decreasing Δf. In this manner the beat-note frequency rapidly decreases toward zero, the VCO frequency drifts toward f_s, and the lock is established. When the system is in lock, Δf is equal to zero and only a steady state dc error voltage remains.

The total time taken by the PLL to establish lock is called the "pull-in" time. Pull-in time depends on the initial frequency and phase difference between the two signals, as well as on the overall loop gain and the low-pass filter bandwidth. Under certain conditions, the pull-in time may be shorter than the period of the beat-note; and the loop can lock without an oscillatory error transient.

In the operation of the loop, the low-pass filter serves a dual function: first, by attenuating the high frequency error components at the output of the phase comparator, it enhances the interference rejection characteristics;

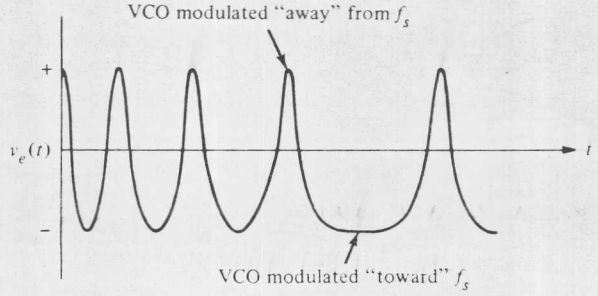


Figure 9.16 Asynchronous error beat-note during capture process.

secondly, it provides a short-term memory for the PLL and ensures a rapid recapture of the signal if the system is thrown out of lock due to a noise transient. Since the low-pass filter attenuates the high-frequency error voltage within the loop, it directly controls the capture and the transient-response characteristics of the PLL. The reduction of the filter bandwidth has the following effects on system performance:

1. The capture process becomes slower, and the pull-in time increases.
2. The capture range decreases.
3. Interference rejection properties of the PLL improve since the error voltage caused by an interfering frequency is attenuated further by the low-pass filter.
4. The transient response of the loop, i.e., the response of the PLL to sudden changes of the input frequency within the capture range, becomes underdamped.

The last point also brings about a practical limitation of the low-pass loop filter bandwidth and roll-off characteristics from stability considerations. These points will be explained further in the following section.

9.11 BASIC DESIGN PARAMETERS FOR A PLL SYSTEM

The phase-locked loop exhibits frequency selective response characteristics centered about the VCO free-running frequency. The two parameters which describe the selectivity characteristics are the "lock" and the "capture" ranges defined in the preceding section. These characteristics can be readily related to the parameters of the individual blocks shown in Fig. 9.15. The time dependence of the phase error $\phi_e(t)$ can be expressed by the following differential equation:[26]

$$d\phi_o/dt = K_o K_d A_1[f(t)^* \sin \phi_e] \tag{9.47}$$

where the asterisk denotes convolution and,

K_o = VCO voltage to frequency conversion gain in radians per volt/second.

K_d = conversion gain of phase comparator (in volts/radian)

$f(t)$ = impulse response of the low-pass filter

The sine ϕ_e dependence in Eq. (9.47) comes about because most practical phase-comparator circuits have an output voltage which is proportional to either the sine or the cosine of the phase error (see Eq. 7.45).

Even for a simple one-pole low-pass loop filter, Eq. (9.47) leads to a nonlinear second-order differential equation, and cannot be solved in a closed form. The lock range, $\Delta\omega_L$, corresponds to the maximum value of

$(d\phi_o/dt)$ for which a steady state solution of (9.47) is possible. Assuming unity dc gain for the low-pass filter, one can show that[25]

$$\Delta\omega_L = K_o K_d A_1 = \text{total dc loop gain} \tag{9.48}$$

Since the capture range $\Delta\omega_c$ denotes a transient condition, it is not as readily derived as the lock range. However, an approximate parametric expression for the capture range can be written as[27]

$$\Delta\omega_c \approx K_o K_d A_1 |F(j\Delta\omega_c)| \tag{9.49}$$

where $|F(j\Delta\omega_c)|$ is the low-pass filter amplitude response at $\omega = \Delta\omega_c$. It should be noted that, since at all times $|F(j\Delta\omega_c)| \leq 1.0$, the capture range is always smaller than the lock range. If a simple lag filter is used (see Fig. 9.18(*a*)) the capture range equation can be approximated as

$$\Delta\omega_c \approx \sqrt{\frac{\Delta\omega_L}{\tau_1}} \tag{9.50}$$

where τ_1 is the low-pass filter time constant.

From Eqs. (9.48) and (9.49), it is seen that the gain A_1 of the dc amplifier within the loop provides an independent means of controlling the loop gain, and the lock range. Similarly, for a given value of the loop gain, the capture range is set by the choice of low-pass filter response $F(j\omega)$.

When the PLL is in lock, nonlinear capture transients are no longer present. Therefore, under lock condition, it can be approximated as a linear control system, as shown in Fig. 9.17, and can be analyzed using Laplace transform techniques. In this case, it is convenient to use the net phase error within the loop as the system variable, with ϕ_s and ϕ_o denoting the relative phase between the signal input and the VCO output. Note that since the VCO converts a voltage to a frequency, and since phase is the integral of frequency, the VCO functions as an integrator in the feedback loop. In the linear model of Fig. 9.17, it is assumed that the net phase shift $(\phi_o - \phi_s)$ is sufficiently small such that

$$\sin(\phi_o - \phi_s) \approx \phi_o - \phi_s \tag{9.51}$$

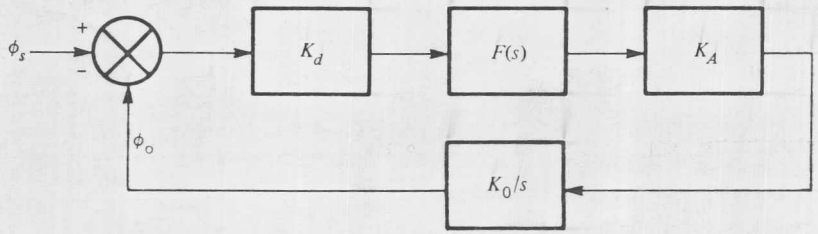


Figure 9.17 Linearized model of the PLL as a negative feedback system.

From the Figure, the open loop transfer function for the PLL can be written as

$$T(s) = \frac{K_T F(s)}{s} \tag{9.52}$$

where K_T is the total loop gain ($K_T = K_o K_d A_1$) and $F(s)$ is the low-pass filter transfer function. Using linear feedback analysis techniques, the closed-loop transfer characteristics $H(s)$ can be related to the open-loop performance as

$$H(s) = \frac{\phi_o(s)}{\phi_s(s)} = \frac{T(s)}{1 + T(s)} \tag{9.53}$$

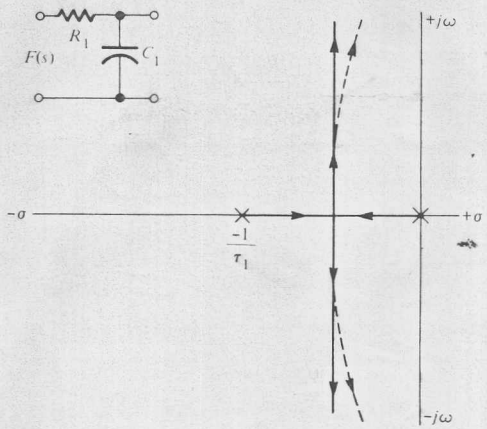
and the roots of the characteristic system polynomial can be readily determined by root-locus techniques. Figure 9.18 shows the PLL root-loci for the linearized model of Fig. 9.17, as a function of increasing loop gain K_T for single-pole lag and lag-lead type filters. In each case, the open-loop pole at the origin is due to the integrating action of the VCO.

With reference to the root-locus characteristics of Fig. 9.18(*a*), one can make the following observations:

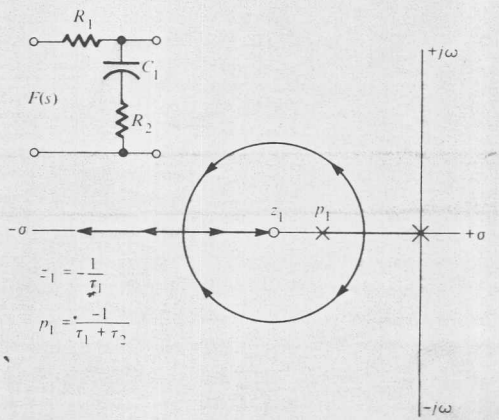
1. As the loop gain K_T increases, for a given choice of τ_1, the imaginary part of the closed-loop poles increases; thus, the natural frequency of the loop increased and it becomes more and more under damped.
2. If the filter time constant τ_1 is increased, the real part of the closed-loop poles becomes smaller, and the loop damping is reduced.

As in any practical feedback system, excess phase shifts or non-dominant poles associated with the blocks within the PLL can cause the loci to bend toward the right-half plane, as shown by the dotted lines in 9.18(*a*). This is likely to happen if either the filter time constant or the loop gain is too large, and can cause the loop to break into sustained oscillations. The stability problem can be eliminated by using a lag-lead type filter as shown in 9.18(*b*). By proper choices of R_2 this type of filter confines the root-locus to the left-half plane and ensures stability. However, this type of filter also reduces the interference rejection characteristics of the system since the high frequency error components within the loop are now attenuated to a lesser degree.

When the PLL is in lock, a frequency shift at the input is transferred to a voltage level shift at the VCO control terminal. Figure 9.19 shows the typical frequency-to-voltage transfer characteristics of the PLL. The input is assumed to be a sine-wave whose frequency is swept slowly over a broad frequency range; and the vertical scale is the corresponding loop error voltage. In the top Figure the input frequency is being gradually increased. The loop does not respond to the signal until it reaches a frequency f_1,



(a) Lag filter: $F(s) = \dfrac{1}{1 + s\tau_1}$



(b) Lag-lead filter: $F(s) = \dfrac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}$

Figure 9.18 PLL root-locus for various low-pass filters.

corresponding to the lower edge of the capture range. Then, the loop suddenly locks on the input, causing a negative jump of the loop error voltage; as the input frequency is increased further V_d varies with frequency with a slope equal to the reciprocal of VCO gain ($1/K_0$) and goes through zero as $f_s = f_o$. The loop tracks the input until the input frequency reaches f_2, corresponding to the upper edge of the lock range. Then the PLL loses lock, and the error voltage drops to zero, and the VCO frequency returns to f_o. If the input frequency is now swept slowly back, the cycle repeats

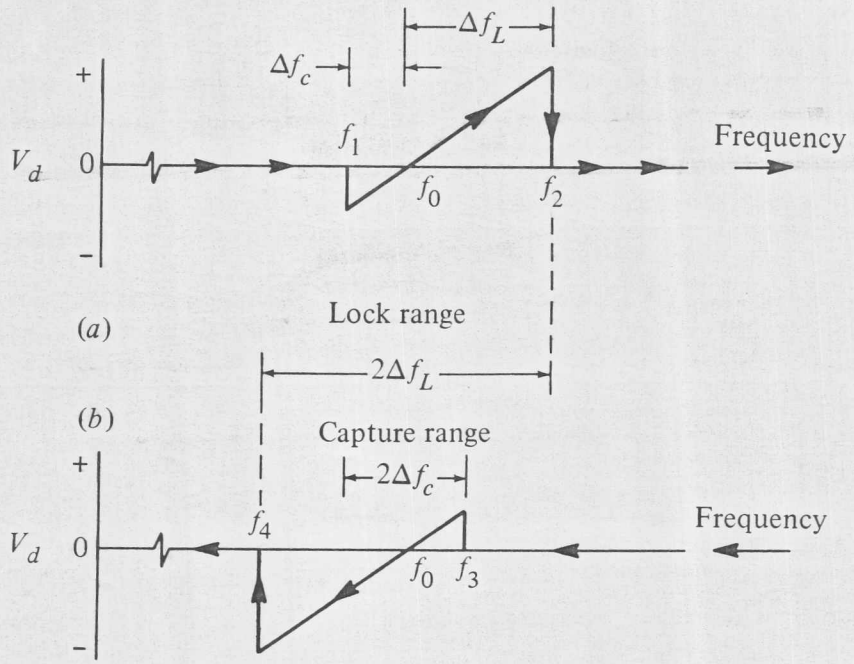


Figure 9.19 Typical PLL frequency-to-voltage transfer characteristics: (*a*) slowly increasing input frequency; (*b*) decreasing frequency.

itself as shown in Fig. 9.19(*b*). The loop recaptures the signal of f_3 and traces it down to f_4. The frequency spread between (f_1, f_3) and (f_2, f_4) corresponds to the total capture and lock ranges of the system, i.e.,

$$f_3 - f_1 = 2\Delta f_C \qquad \text{and} \qquad f_2 - f_4 = 2\Delta f_L \tag{9.54}$$

Note that, as indicated by the transfer characteristics of Fig. 9.19, the PLL system has an inherent selectivity about the center frequency set by the VCO free-running frequency, f_0; and it would only respond to the input signal frequencies which are separated from f_0 by less than Δf_C or Δf_L, depending on whether the loop starts with or without an initial lock condition. It is also worth noting that the linearity of the frequency-to-voltage conversion characteristics for the PLL are solely determined by the VCO conversion gain. Therefore, in most applications, the VCO is required to have a highly linear voltage-to-frequency transfer characteristic.

9.12 APPLICATIONS OF A PLL

The phase-locked loop is a versatile system block which is suitable for a variety of frequency selective demodulation, signal conditioning, or fre-

quency synthesis applications. Some of these basic applications are briefly described below:

1. FM Demodulation

If the PLL is locked on a frequency modulated (FM) signal, the VCO tracks the instantaneous frequency of the input. Then the filtered error voltage $v_d(t)$, which constrains the VCO to maintain lock with the input signal, corresponds to the demodulated output. In this case, the linearity of the demodulated output is determined by the VCO voltage-to-frequency conversion characteristics (see Fig. 9.19). The PLL can be used for detecting either wide-band (high deviation) or narrow-band FM signals with a higher degree of linearity than can be obtained by other FM detection means. It is worth noting that for FM deviation purposes, the PLL functions as a self-contained receiver system since it combines the functions of frequency selection and demodulation.

In the case of frequency-shift keyed (FSK) data transmission, the digital information is transmitted by switching the input frequency between any one of the two discrete input frequencies, corresponding to a digital "one" and a digital "zero," respectively. When the PLL is locked on an FSK input signal, the error voltage $v_d(t)$, which is in the form of discrete voltage steps, corresponds to the demodulated binary output.

It should be noted that since the PLL is in lock during the FM demodulation process, the frequency response as well as the rise time of the demodulated output can be readily predicted from the root-locus plots of Fig. 4.18.

2. Frequency Synchronization

Using the phase-locked loop system, the frequency of a relatively poor oscillator such as the VCO can be phase-locked with a low level but highly stable reference signal. Then, the VCO output reproduces the input signal frequency at the same per-unit accuracy as the input reference, but at a much higher power level. In some applications, the synchronizing signal can be in the form of a low duty cycle burst at a specific frequency. Then the PLL can be used to regenerate a coherent CW reference frequency, by locking on this short synchronizing pulse. A typical example of such an application is the phase-locked chroma-reference generators in color TV receivers.

In digital systems, the PLL can be used for a variety of synchronization functions. For example, two system clocks can be phase-locked to each other such that one can function as a backup for the other; or it can

be used in synchronizing disc or tape drive mechanisms in information storage and retrieval systems. In pulse-code modulation (PCM) telemetry receivers or in repeater systems, the PLL is used for bit synchronization.

3. Signal Conditioning

By proper choice of the VCO free-running frequency, the PLL can be made to lock on any one of a number of signals present at the input. Then the VCO output reproduces the frequency of the desired signal while greatly attenuating the undesired frequencies or side bands present at the input. If the loop bandwidth is sufficiently narrow, the signal-to-noise ratio at the VCO output can be much higher than that at the input. Thus the PLL can be used as a noise filter for regenerating weak signals buried in noise.

4. Frequency Multiplication and Division

By inserting a frequency divider into the feedback loop, between the VCO output and the phase comparator input, the PLL system can function as a frequency-selective frequency multiplier. A block diagram of this configuration is shown in Fig. (9.20) where N is the frequency divider modulus.

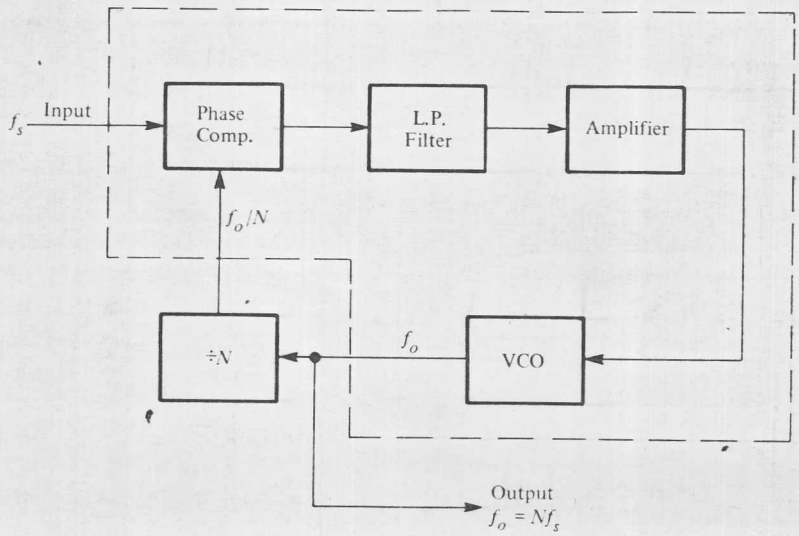


Figure 9.20 Frequency multiplication by using a frequency divider in PLL feedback loop.

When the system is in lock, the two inputs to the phase comparator are at the same frequency, and $f_o = Nf_s$.

Under certain conditions, frequency multiplication can also be achieved without the use of a frequency divider network, by operating the PLL in its "harmonic-locking" mode. The principle of harmonic-lock can be briefly explained as follows: If the VCO output is nonsinusoidal, it will contain a number of harmonics in addition to its fundamental frequency. In other words, the output of a nonsinusoidal VCO is effectively a composite signal containing frequency components at integral multiples of VCO fundamental frequency. The same is also true for a nonsinusoidal input signal, such as a pulse train. If the VCO free-running frequency is set to be close to the n^{th} harmonic of a harmonic-rich input signal, the VCO fundamental can be made to synchronize with the n^{th} harmonic of the input. Then, under this condition, the PLL operates in a harmonic-lock mode, and the VCO frequency is exactly n times the input frequency, or $f_o = nf_s$.

Similarly, if the VCO produces a harmonic-rich output waveform, the m^{th} harmonic of the VCO output can be synchronized with the input fundamental. Then, under this condition, the VCO fundamental is a subharmonic of the input frequency, i.e., $f_o = f_s/m$. When the PLL is operated in the harmonic-locking mode, the spacing between the adjacent harmonics in the frequency spectrum decreases rapidly as the harmonic order n or m is increased. This in turn, increases frequency stability requirements for the VCO free-running-frequency, to enable the system to differentiate between adjacent harmonics. In integrated phase-locked loop systems which use multivibrator type oscillators,[28] thermal drifts of VCO frequency usually restrict the harmonic-lock operation of the system to values of n or $m \leq 10$. An additional disadvantage of harmonic-locking at large values of n or m is that the phase-detector gain K_d decreases inversely with the harmonic order, thus decreasing both the lock and the capture ranges of the system at higher harmonics.

5. Frequency Translation

The PLL system can be used to translate the frequency of a highly stable but fixed frequency reference oscillator by a small amount in frequency. This can be achieved by adding a mixer and a low-pass filter stage to the basic PLL, as shown in Fig. (9.21). In this case, the reference input f_R and the VCO input f_o are applied to the inputs of the mixer stage. The mixer output is made up of the "sum" and the "difference" components of f_o and f_R. The sum component is filtered by the first low-pass filter. The translation or offset frequency f_1 is applied to the phase comparator, along with

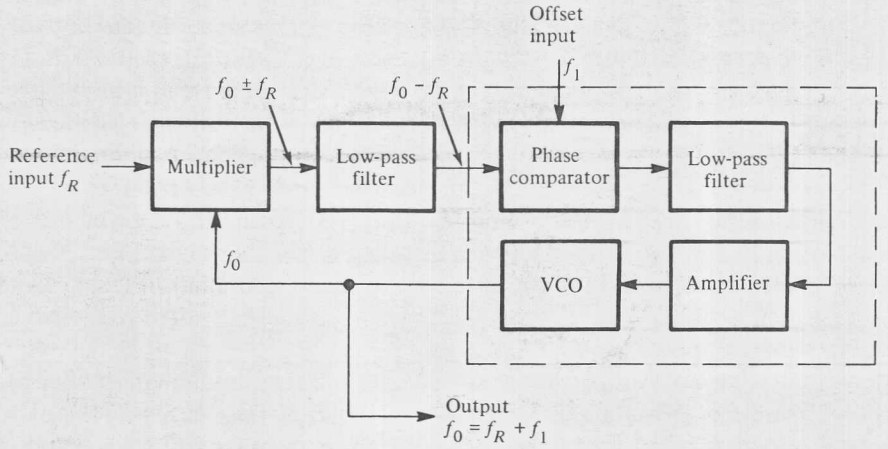


Figure 9.21 Frequency translation or "frequency-offset" loop.

the $f_R - f_o$ component of the mixer output. When the system is in lock, the two inputs of the phase comparator are at identical frequency, i.e.,

$$f_0 - f_R = f_1 \qquad \text{or} \qquad f_0 = f_R + f_1 \tag{9.55}$$

6. AM Detection

The PLL can be used as a coherent detector for demodulating amplitude modulated (AM) signals. In this mode of operation, the PLL locks on the carrier of the AM signal and produces a reference signal at the output of the VCO, which has the same frequency as the AM carrier, but no amplitude modulation. Then, by multiplying this coherent reference signal with the modulated input signal and low-pass filtering the output of the multiplier, one can obtain the demodulated information. A block diagram of such a system is shown in Fig. (9.22). Since the PLL only responds to

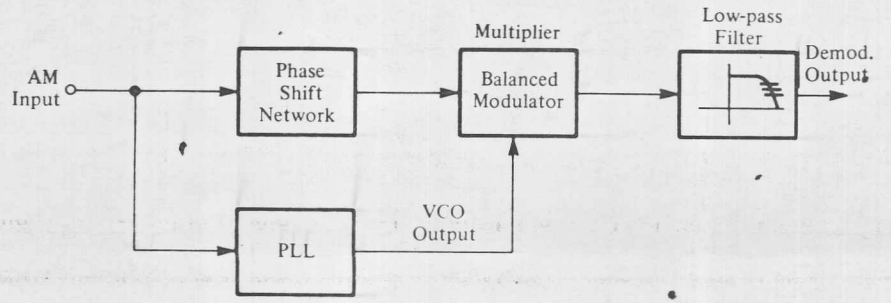


Figure 9.22 Coherent AM detection using a phase-locked loop.

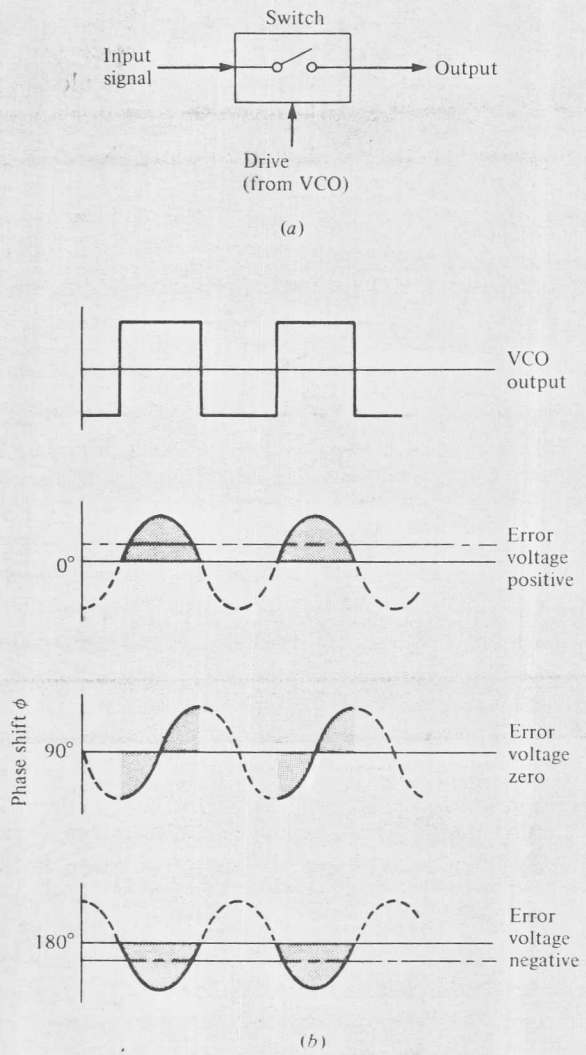


Figure 9.23 Operation of a switch-type phase detector: (*a*) block diagram; (*b*) typical waveforms.

PLL system using this type of a phase comparator when the PLL is in perfect lock condition (i.e., $v_d(t) = 0$), the VCO output is at quadrature phase with the input.

The switch-type phase comparator circuits can be readily derived from the balanced modulator circuits discussed in Chapter 7 (see Sections 7.5 and 7.6). Figures 7.3 and 7.10 show two balanced modulator configura-

carrier frequencies very close to VCO frequency f_o the phase-locked AM detector system also exhibits a high degree of selectivity, cntered about f_o.[29] The phase-shift network shown in the block diagram of Fig. (9.22) is a noncritical RC network which is used to offset the 90° phase shift introduced by the PLL. The reason for this phase shift will be described in the following section.

The phase-locked AM detection method shown in Fig. (9.22) is a coherent detection technique; therefore, it offers a higher degree of noise immunity than conventional peak-detector type AM dmodulators.

9.13 BUILDING BLOCKS FOR A MONOLITHIC PLL

Each of the basic blocks forming the PLL system of Fig. 9.15 can be readily integrated in monolithic form, with present-day IC technology. Therefore the entire PLL system itself is well suited to integration. The key blocks which determine the characteristics of the system are the phase comparator and th VCO sections. In this section some basic circuit configurations will be described for the VCO and the phase comparator sections. These particular circuit topologies are chosen because they are readily compatible with monolithic bipolar technology; and their operations rely mainly on the matching and the thermal tracking of monolithic components, rather than on the tight control of absolute value tolerances.

1. The Phase Comparator

The simplest phase comparator circuit suitable for monolithic integration is the switch-type phase detector which is shown schematically in Fig. 9.23(*a*) This type of a detector operates as a synchronous switch which is opened and closed by the reference input, and effectively "chops" the signal input, at the same repetition rate as the reference drive. Normally, the reference drive is supplied by the VCO output.

Figure 9.23(*b*) shows the typical output waveforms for the switch-type phase comparator, for a sinusoidal input and a square-wave drive signal. The filtered error voltage V_d corresponds to the average value of the output waveform, and is shown as the shaded area in the waveforms. The error voltage is zero when the net phase shift ϕ_n between the two inputs is 90°. This 90° phase shift is a common property of all switch-type phase comparator circuits, and results in a comparator gain expression of the form,

$$K_d = K_A \cos \phi_n \tag{9.56}$$

where K_A is a constant of proportionality at a given input signal level. In a

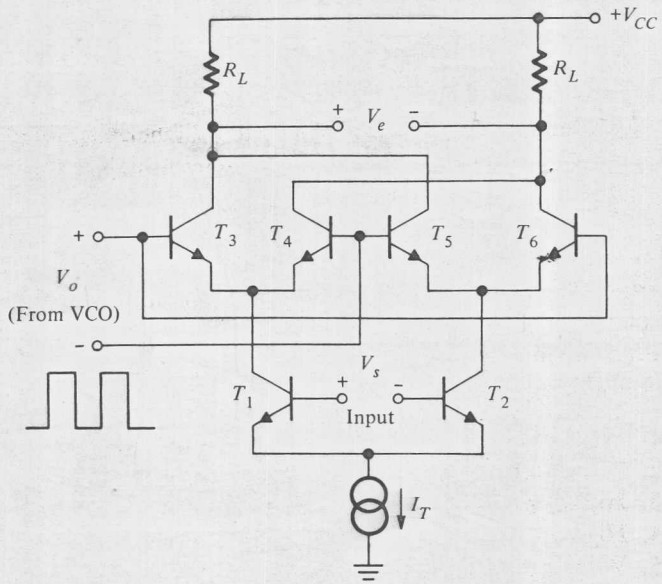


Figure 9.24 A phase comparator circuit based on the balanced modulator configuration.

tions suitable for monolithic integration. The circuit of Fig. 7.3 is normally preferred over that of Fig. 7.10 since it provides higher conversion gain and can be built with all bipolar transistors.[30]

Figure 9.24 shows the balanced modulator circuit of Fig. 7.3 in phase comparator application. In this circuit, the input signal $v_s(t)$ is applied to the bases of T_1 and T_2, and controls the partitioning of bias current between these two devices. The high-level VCO output is applied to cross-coupled transistor pairs (T_3, T_4) and (T_5, T_6); and causes these devices to function as two sets of single-pole double-throw switches actuated by the VCO waveform. If $v_s(t)$ and $v_o(t)$ are at the same frequency, the dc output voltage V_e is related to the phase difference ϕ_o between the two signals as

$$V_e = \frac{g_m R_L E_s}{\pi} \cos \phi_o \tag{9.57}$$

where g_m is the transconductance of T_1 or T_2, and E_s is the amplitude of $v_s(t)$.

The low-pass filter can be readily incorporated into the phase-comparator circuit of Fig. 9.24 by connecting a series combination of a capacitor C_1 and resistor R_2 across the output terminals of the phase detector. This results in a low-pass filter function, $F(s)$, given as

In an actual design, this low-pass filter would normally be left external to the monolithic circuit, to facilitate a higher degree of flexibility.

2. The Voltage Controlled Oscillator

In the design of a PLL the voltage-controlled oscillator is usually the most critical block since the frequency stability and the FM demodulation characteristics of the system are normally determined by the VCO performance. For maximum versatility, the VCO is required to have the following desirable properties:

1. Linear voltage to frequency conversion.
2. Good frequency stability (low thermal and long term drift).
3. High frequency capability.
4. High voltage-to-frequency conversion gain.
5. Wide tracking range.
6. Ease of tuning (frequency of oscillation determined by a minimum number of circuit components).

In addition to these requirements, to be suitable for monolithic integration, the VCO circuit should contain no inductors.

Figures 9.25 and 9.26 show two basic oscillator configurations which fulfill most of the requirements listed above. The circuit of Fig. 9.25 is an integrator and Schmitt-trigger combination where the timing capacitor C_o is alternately charged and discharged by a voltage controlled current source I_1.[31] The Schmitt trigger, comprised of T_4 through T_7, senses the voltage level V_A across C_o and turns the switch transistor T_3 off or on to initiate the charge and discharge cycles, respectively. The frequency of oscillation f_o can be expressed as

$$f_o = \frac{V_c g_m}{2\, C_o(V_2 - V_1)} \tag{9.59}$$

where g_m is the transconductance of the voltage-controlled current source, and V_2 and V_1 are the upper and lower trip levels for the Schmitt trigger. This type of an oscillator can provide either a triangular-wave (at node A) or a square-wave (at node B) output. Note that transistors T_1 and T_2 form a diode-connected current sink (see Fig. 4.2) and thus force the charging and the discharging currents to be equal. This results in a 50 percent duty cycle of the VCO output waveform. In the actual design of the VCO circuit of Fig. 9.25, the voltage-controlled current source can be designed using any one of the circuit configurations discussed in Chapter 4 (see Figs. 4.17

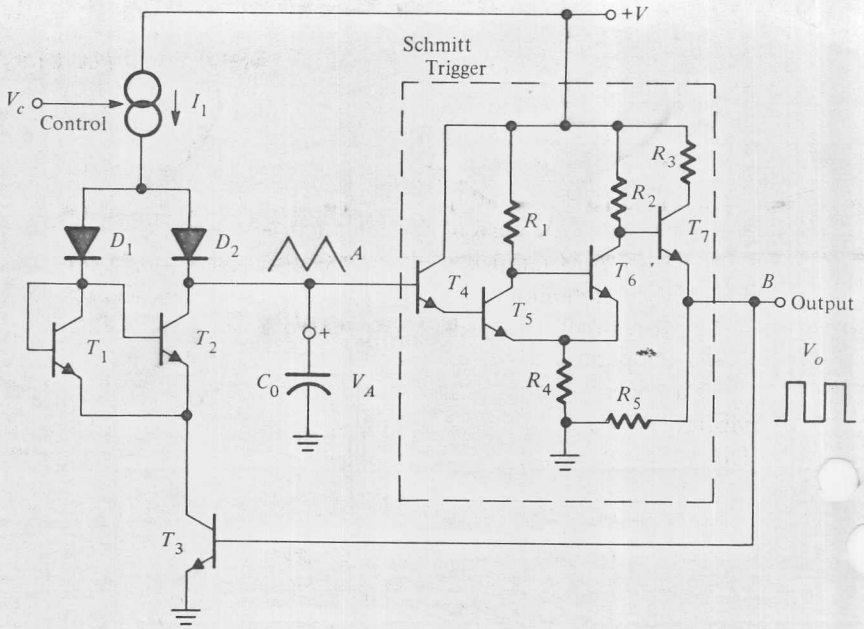


Figure 9.25 A voltage-controlled oscillator using an integrator and Schmitt-trigger combination.

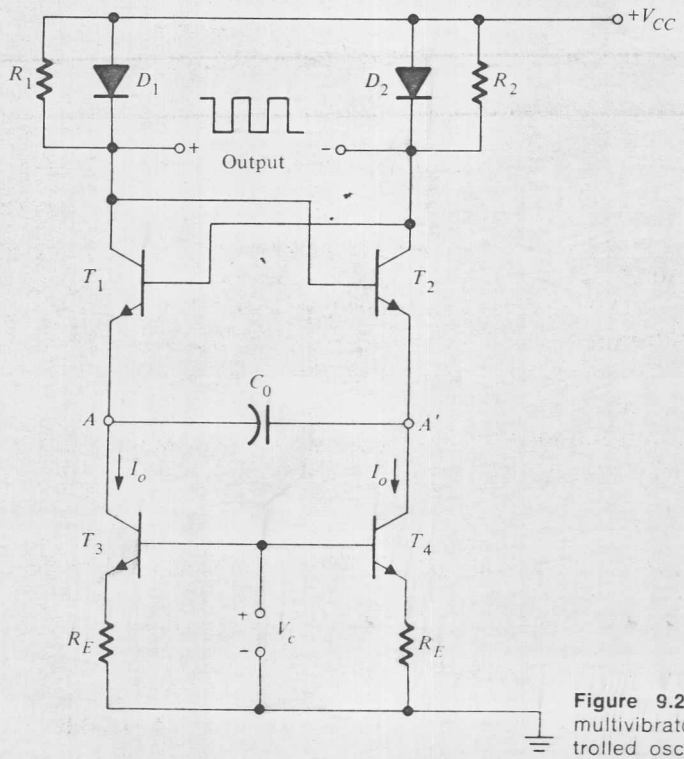


Figure 9.26 An emitter-coupled multivibrator type voltage-controlled oscillator.

and 4.18) with an external resistor used to set the bias current level I_1, for zero control voltage. Since the current source uses a *pnp* transistor, the high frequency capability of the circuit is somewhat limited ($f_o \leq 1$ MHz). However, since the current I_1 and switching levels V_1 and V_2 can be made to have very low temperature coefficients using the matching and thermal-tracking of monolithic components, this type of an oscillator offers a high degree of temperature stability (typically $\partial f_o/\partial T < \pm 200$ ppm/°C) over a broad temperature range.

The VCO circuit of Fig. 9.26 is basically an emitter-coupled multivibrator, with cross-coupled transistors T_1 and T_2 forming the positive feedback gain stage.[32] At any one time, either T_1 or T_2 is on and the timing capacitor C_o is alternately charged and discharged by a constant current I_o provided by the voltage-controlled current sources T^3 and T_4. The frequency of oscillation can be expressed as

$$f_o = \frac{I_o}{4\, C_o V_{BE}} \tag{9.60}$$

where V_{BE} is the transistor base-emitter voltage. Diodes D_1 and D_2 clamp the output swing to one V_{BE} drop below the positive supply voltage, and make the output amplitude independent of the control voltage. The circuit provides a balanced square-wave output across diodes D_1 and D_2. The conversion gain K_o can be written as

$$K_o = \frac{1}{4\, C_o R_E V_{BE}} \text{ Hz/V} \tag{9.61}$$

Since the VCO of Fig. 9.26 is a nonsaturating circuit using all *npn* transistors, it offers higher frequency capability than that of Fig. 9.25, and can operate up to 60 MHz. As shown by Eq. 9.60, the frequency of the emitter-coupled VCO is inversely proportional to V_{BE}, which has a strong negative temperature coefficient ($\partial V_{BE}/\partial T \approx -2$mV/°C or ≈ -3000 ppm/°C). In the actual VCO design, this temperature drift can be compensated by introducing an equal temperature dependence on the current I_o so as to keep the ratio (I_o/V_{BE}) independent of temperature. Using this type of compensation, the temperature coefficient of f_o can be kept as low as ± 400 ppm/°C over a temperature range of -55 to $+125$°C.[28]

It should be noted that both of the VCO circuits described in this section offer linear control characteristics (i.e., f_o proportional to V_c) and can be tuned to any desired frequency by means of a single timing capacitor C_o.

9.14 A MONOLITHIC PLL SYSTEM

The basic blocks described in the previous section can be readily fabricated and interconnected in monolithic form, to function as a self-

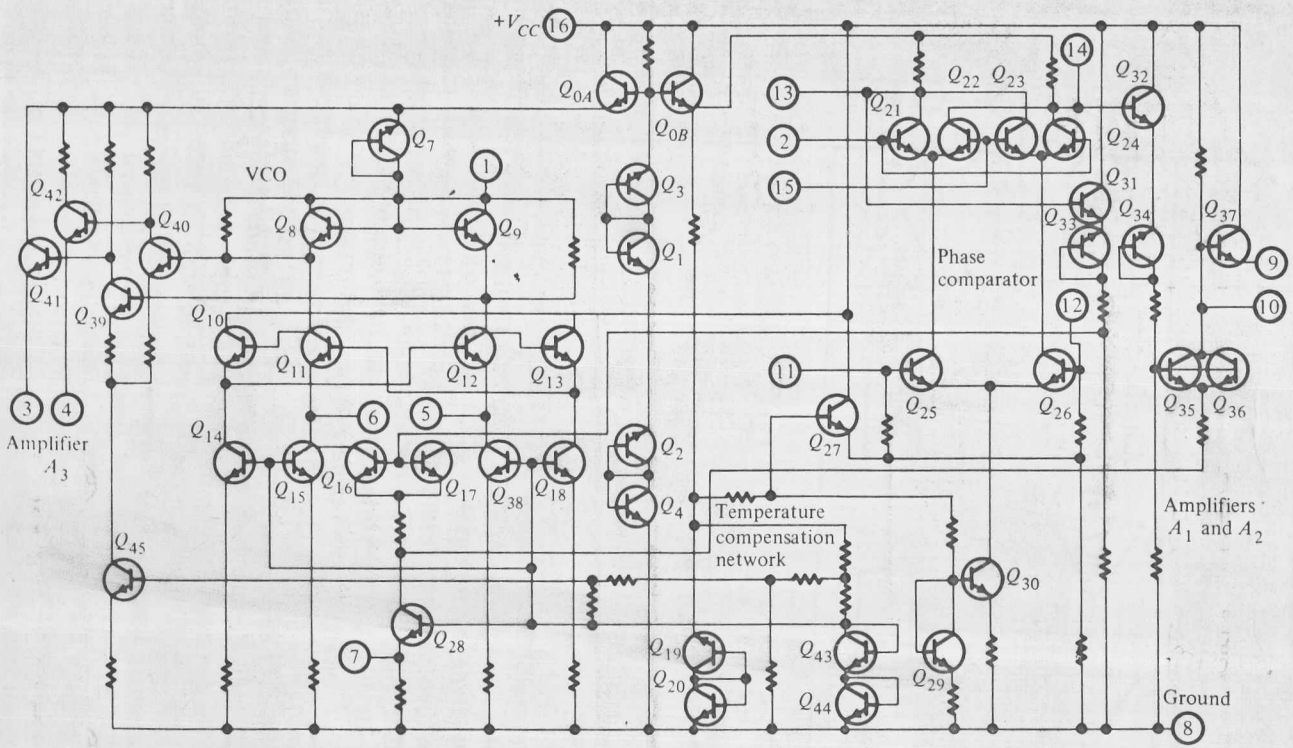


Figure 9.27 Circuit schematic of a monolithic PLL system.[28]

phase-locked feedback loop is not internally connected. Instead, the loop is opened between the VCO and the phase comparator inputs so that either a divide-by-n circuit or a mixer circuit can be inserted into the loop for frequency-multiplication or frequency-translation applications (see Figs. 9.20 and 9.21). In addition to the basic blocks necessary to form the PLL, the monolithic system also contains two additional amplifiers A_2 and A_3. A_2 is used as a buffer amplifier to increase the demodulated output level for FM or FSK detection; A_3 amplifies the VCO output signal and provides digital interface capability with conventional logic circuits. A limiter

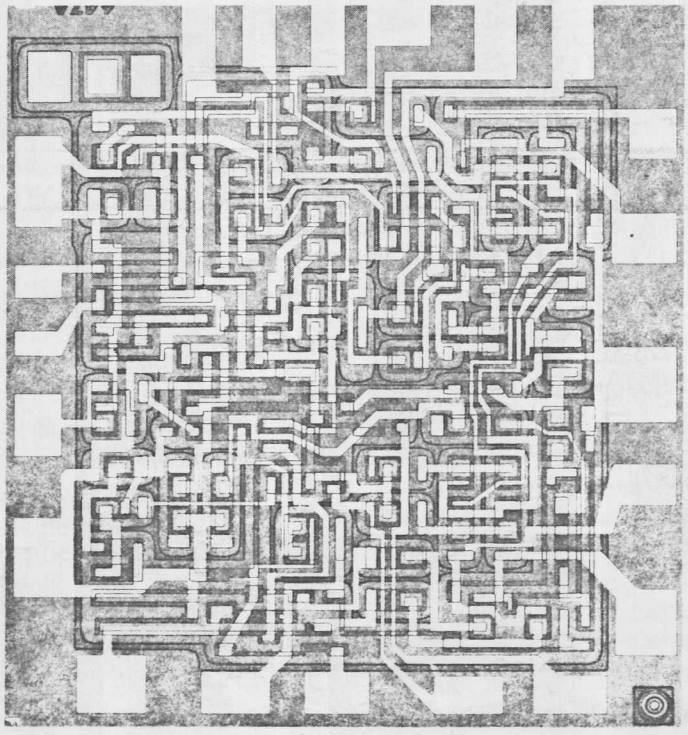


Figure 9.29 Topological layout of the PLL circuit chip size: 67 × 72 mils. *(Photo: Signetics.)*

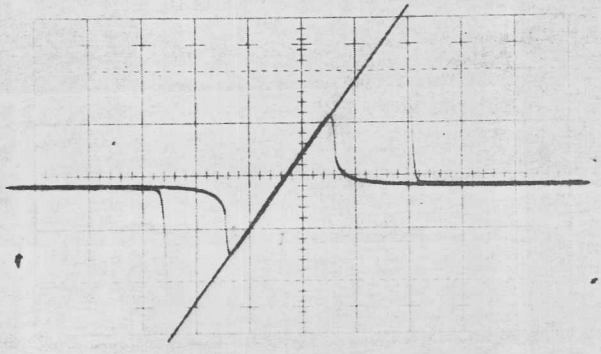


Figure 9.30 Oscillogram of PLL frequency-to-voltage transfer characteristics at f_0 = 10 MHz. (Scale: vertical = 0.5 V/division, horizontal = 500 kHz/division.)